METHOD AND SYSTEM FOR PLANAR REGROWTH IN GAN ELECTRONIC DEVICES

BACKGROUND OF THE INVENTION

[0001] Power electronics are widely used in a variety of applications. Power electronic devices are commonly used in circuits to modify the form of electrical energy, for example, from ac to dc, from one voltage level to another, or in some other way. Such devices can operate over a wide range of power levels, from milliwatts in mobile devices to hundreds of megawatts in a high voltage power transmission system. Despite the progress made in power electronics, there is a need in the art for improved electronics systems and methods of operating the same.

SUMMARY OF THE INVENTION

[0002] The present invention relates generally to electronic devices. More specifically, the present invention relates to devices with substantially planar regrown regions. Merely by way of example, the invention has been applied to methods and systems for the selective regrowth of planar gallium-nitride (GaN) based epitaxial layers. The methods and techniques can be applied to a variety of compound semiconductor systems including vertical junction field effect transistors (JFETs), electrical contact structures, diode structures, and the like.

[0003] According to an embodiment of the present invention, a method for fabricating an electronic device is provided. The method includes providing a III-nitride substrate and forming a III-nitride epitaxial layer coupled to the III-nitride substrate. The III-nitride epitaxial layer has an upper surface and a thickness. The method also includes removing a predetermined portion of the III-nitride epitaxial layer to form one or more recessed regions extending from the upper surface to a predetermined depth into the III-nitride epitaxial layer and regrowing a III-nitride epitaxial material in the one or more recessed regions. The III-nitride epitaxial material has an upper regrowth surface substantially coplanar with the upper surface of the III-nitride epitaxial layer.

[0004] According to another embodiment of the present invention, a vertical JFET is provided. The vertical JFET includes a III-nitride substrate and a III-nitride epitaxial layer of a first conductivity type coupled to the III-nitride substrate. The first III-nitride epitaxial layer has a first dopant concentration. The vertical JFET also includes a III-nitride epitaxial structure coupled to the first III-nitride epitaxial layer. The III-nitride epitaxial structure includes a set of channels of the first conductivity type and having a second dopant concentration, a set of sources of the first conductivity type, having a third dopant concentration greater than the first dopant concentration, and each characterized by a contact surface, and a set of regrown gates interspersed between the set of channels. An upper surface of the set of regrown gates is substantially coplanar with the contact surfaces of the set of sources.

[0005] According to a specific embodiment of the present invention, a method of fabricating a vertical JFET is provided. The method includes providing a III-nitride substrate and forming a first III-nitride epitaxial layer of a first conductivity type coupled to the III-nitride substrate. The first III-nitride epitaxial layer has a first thickness. The method also includes forming one or more additional III-nitride epitaxial layers coupled to the first III-nitride epitaxial layer and removing a portion of the one or more additional III-nitride epitaxial layers to form a set of recesses extending a predetermined distance into the one or more additional III-nitride epitaxial layers. The set of recesses are disposed between remaining portions of the one or more additional III-nitride epitaxial layers. The method further includes regrowing an epitaxial material in the set of recesses. The epitaxial material has a thickness substantially equal to the predetermined distance. Additionally, the method includes forming a drain contact electrically coupled to the III-nitride substrate, forming a set of source contacts electrically coupled to the remaining portions of the one or more additional III-nitride epitaxial layers, and forming a set of gate contacts electrically coupled to the epitaxial material.

[0006] Numerous benefits are achieved by way of the present invention over conventional techniques. For example, embodiments of the present invention utilize an epitaxial regrowth process to produce planar device surfaces, improving lithography resolution and device yield. Additionally, embodiments of the present invention maximize active area and current-handling capability of electronic devices as well as improve yield and reliability. These and other embodiments of the invention, along with many of its advantages and features, are described in more detail in conjunction with the text below and attached figures.

BRIEF DESCRIPTION OF THE DRAWINGS

[0007] FIG. **1** is a simplified cross-sectional diagram illustrating a vertical JFET according to an embodiment of the present invention;

[0008] FIGS. **2**A-**2**D are simplified cross-sectional diagrams illustrating the fabrication of a vertical JFET according to an embodiment of the present invention;

[0009] FIG. **3** is a simplified schematic diagram illustrating a planar regrown contact structure according to an embodiment of the present invention;

[0010] FIG. **4** is a simplified schematic diagram illustrating a planar regrown resistor structure according to an embodiment of the present invention;

[0011] FIG. **5** is a simplified flowchart illustrating a method of fabricating an electronic device according to an embodiment of the present invention; and

[0012] FIG. **6** is a simplified flowchart illustrating a method of fabricating a vertical JFET with regrown gate regions according to an embodiment of the present invention.

DETAILED DESCRIPTION OF SPECIFIC EMBODIMENTS

[0013] Embodiments of the present invention relate to electronic devices. More specifically, the present invention relates to devices with substantially planar regrown regions. Merely by way of example, the invention has been applied to methods and systems for the selective regrowth of planar gallium-nitride (GaN) based epitaxial layers. The methods and techniques can be applied to a variety of compound semiconductor systems including vertical junction field effect transistors (JFETs), electrical contact structures, diode structures, and the like.

[0014] GaN-based electronic and optoelectronic devices are undergoing rapid development. Desirable properties associated with GaN and related alloys and heterostructures include high bandgap energy for visible and ultraviolet light